PVP 14

Code: EC5T5

III B.Tech - I Semester – Regular/Supplementary Examinations
October 2019

DIGITAL IC APPLICATIONS
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) Write the example of Case statement of Verilog HDL.

   b) Define assignment statement.

   c) Compare two advantages of CMOS over TTL logic family.

   d) Draw the logic symbols of 74XX139 and 74XX138.

   e) Prepare the logic symbol of Non-inverting Tri-state buffer.

   f) Write the Verilog model of 2 I/P AND gate.

   g) What are impediments in Synchronous design?

   h) Compare two major aspects of Latch and Flip-Flop.

   i) Expand EPROM and EEPROM.

   j) What is the number of address lines required for 2^n word lines of PROM?

   k) Write the characteristics table of JK Flip-Flop.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Write the Syntax of a Verilog module declaration. 3 M

b) Interpret the key words to specify the signal direction in Verilog. 3 M

c) Compare Combinational and Sequential logic designs. 10 M

3. a) Design a CMOS 2 I/P NOR gate and verify its function table. 8 M

b) Analyze Sinking current and Sourcing current of TTL gate. Which of the parameters decide the fan-out and how? 8 M

4. a) Design a combinational circuit for the function

$$F(A,B,C)= \sum m(1,2,3,7) + d(0,4)$$

and write the Verilog Program in data flow model. 6 M

b) Construct 3-Bit Binary to Gray code converter and write the Verilog code for the same. 10 M

5. a) Model the Verilog code for D-Flip flop using behavioural modeling style. 6 M

b) Construct 3-bit up/down ripple counter using mode control input. 10 M

6. a) Identify the necessity of two-dimensional decoding mechanism in memories. 4 M

b) Draw MOS transistor memory cell in ROM and explain the operation. 6 M

c) Calculate the number of Address lines, Word lines and Data lines required for 1024 bit memory. 6 M